IN THE SPECIFICATION

Please amend paragraph [0002] on p. 2 as follows:

--Typically, to build software executable on a processor, one or more program files written in a high level programming language, such as, C, C++, ~~Java~~ JAVA, etc., are compiled to generate one or more intermediate files in object code or assembly languages. The intermediate files may then be optionally linked to form an executable.--

Please amend paragraph [0018] on p. 7 as follows:

--A machine-readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine-readable medium includes read only memory ("ROM"); random access memory ("RAM"); magnetic disk storage media; optical storage media; flash memory devices; ~~electrical, optical, acoustical or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.);~~ etc.--

Please amend paragraph [0020] on pp. 7-8 as follows:

--Figure 1A shows a flow diagram of an embodiment of a process to collect addresses of instructions in a software program executed in time order. The process is performed by processing logic that may comprise hardware (e.g., circuitry, dedicated logic, etc.), software (such as is run on a general purpose computer system or a dedicated machine), or a combination of both. The source 101 is in a format, where each instruction is discretely identifiable. The source 101 may be in assembly code, object code, binary code, etc. In contrast, a source that is in a format where the instructions are non-discretely identifiable, such as source 103, has to be converted into a format where individual instructions are discretely identifiable. In one embodiment, the source 101 is derived from a user-created source 103, in which individual instructions are not discretely identifiable. The user-created source 103 may be coded in a high level programming language, such as, C, C++, ~~Java~~ JAVA, etc. In one embodiment, the user-created source 103 is input to the processing block 105 to generate the source 101. The processing block 105 may include a compiler or a linker to generate the source 101. However, one should appreciate that the source 101 may be generated in other manners.--

Please amend paragraph [0022] on pp. 8-9 as follows:

--Figure 1B shows a flow diagram of an embodiment of a process to instrument software. The instrumented software when executed would output the addresses of the instructions in the order in which they are executed. The process is performed by processing logic that may comprise hardware (e.g., circuitry, dedicated logic, etc.), software (such as is run on a general purpose computer system or a dedicated machine), or a combination of both. The individual instructions in the source 101 are discretely identifiable. The source 101 may include assembly code, object code, binary code, etc. In one embodiment, the source 101 is derived from a user-created source 103, which is in a high level programming language, such as, C, C++, ~~Java~~ JAVA, etc. In one embodiment, the user-created source 103 is input to the processing block 105 to generate the source 101. The processing block 105 may include a compiler or a linker to generate the source 101. However, one should appreciate that the source 101 may be generated in other manners.--

Please amend [0026] on pp. 10-11 as follows:

--In one embodiment, an individual codes the ISB in a format where individual instructions are discretely identifiable, such as, for example, in binary code or assembly code. In an alternate embodiment, an individual first codes the ISB in a high level programming language, such as, C, C++, ~~Java~~ JAVA, etc., and then the ISB is converted into another format, such as, assembly code or binary object code, using a tool, such as a compiler, so that each instruction is discretely identifiable. A user may further modify the resulting ISB as appropriate. The exact instructions in the ISB are dependent on the processor that executes the program because each processor may have its own instruction set.--